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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,938	10/31/2001	William B. Connors	10007153-1	4722

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EXAMINER	
NGUYEN, LAM S	

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,938	CONNORS ET AL.	
	Examiner	Art Unit	
	LAM S NGUYEN	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20 and 40* is/are allowed.

6)☒ Claim(s) *1,3-7,9,10,13-16 and 21-26, 28-39* is/are rejected.

7)☒ Claim(s) *2,8 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 36 recites the limitation "the second metal layer" on line 4. There is insufficient antecedent basis for this limitation in the claim. Claims 37-39 are also rejected because they depend on claim 36.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-7, 9-10, 13-16, 21-26, 28-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Kasamoto et al. (US 6056391).

Kasamoto et al. discloses a printhead having a circuit with plural resistors and a power source, comprising:

a metal stack formed within the circuit and comprised of a first/bottom metal layer (*FIG. 1c, element 1110c-b*) comprising a power bus/conductive trace coupled to the power source (*FIG. 1C: The layers 1110c-b are connected to a power source*) and a second/top metal layer comprising a top conductive layer portion and a bottom layer portion (*FIG. 1c, elements 1110a, 1103*), wherein the bottom layer portion has a portion that comprises the resistors (*FIG. 1c, element 1102*) **(Referring to claim 21, 26, 31, 33)**, and

at least one power via (*FIG. 1c, element 1105*) formed within the circuit as an interface between the first metal layer and the second metal layer, wherein, at the power via the second metal layer comprises a separation barrier (*FIG. 1c: The portion of layer 1103 in the area 1105, that is sandwiched between layer 1110c and layer 1110d*) located adjacent the first metal layer (*FIG. 1c, element 1110c*) and between the at least one resistor (*FIG. 1c, element 1102*) of the plural resistors and the power bus (*FIG. 1C: The power is supplied to resistor 1102 relatively through layer 1110c and the separation barrier*), and wherein the second metal layer is connected to the first conductive metal layer portion at the plurality of electrical connection portions (*FIG. 1c, element 1105: The portion of layer 1103 at area 1105*) (**Referring to claims 1, 10, 15, 21-23, 26, 28, 31, 33, 35**).

Referring to claims 3, 16, 24, 29, 34: wherein the circuit is a thin film circuit and the first metal layer is comprised of Aluminum Copper Silicon (*column 5, lines 35-42: "Cu Al-Si alloy"*).

Referring to claims 6, 10, 13, 14: connecting a power bus to the at least one thin film resistor with a power via (*FIG. 1C: The power is supplied to thin film resistor 1102 relatively through the power via 1105)*, and wherein ink corrosion is terminated by the separation barrier at the power/controller via (*column 2, lines 30-45*).

Referring to claims 7, 13, 33: wherein the plural resistors comprise a set of resistors, wherein for the set of resistors, power is routed from the power bus through a plurality of corresponding power/controller vias to each resistor of the set of resistors (*FIG. 1c: The printhead has a plurality of resistors 1102, wherein each resistor 1102 is provided electrical energy through the connection of the electrodes 1110d and 1110a to a corresponding*

power/controller via).

Referring to claim 9: wherein each resistor of the plural resistors is associated with at least one power via that separates metal of the resistor from the power bus (*FIG. 1C: The portion 1105 of the layer 1103 separates the metal layer 1110d to the layer 1110b-c*).

Referring to claims 4-5, 16, 25, 30, 34: wherein the second metal layer is comprised of Aluminum and at least one of Tantalum Aluminum, Tungsten Silicon Nitride, or Tantalum Nitride which provides corrosion resistance and connects the Aluminum to the power bus *column 9, lines 1-3*), wherein a first portion of the Tantalum Aluminum comprises the corresponding at least one of the resistor and a second portion of the Tantalum Aluminum connects the corresponding at least one of the resistor to the power bus (*FIG. 1C*).

Referring to claims 21, 26, 32: a non-metal layer overlying the first metal layer and comprising a via (*FIG. 1c, element 1112: The non-metal layer 1112 comprises the via 1105*), wherein the first metal layer is electrically connected to the electrical connection portion of the bottom layer portion at the via (*FIG. 1c: The first metal layer 1110c is electrically connected to the bottom layer 1103 at the via 1105*), wherein the first metal layer is electrically connected to the first electrical connection portion at the first via and the first metal layer is electrically connected to the second electrical connection portion at the second via (*Fig. 1B-C: The first metal layer 1110c is connected to each of the resistor 1102 through a corresponding via 1105*).\

Allowable Subject Matter

3. Claims 17-20, 40 are allowed claims 2, 8, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 2: The primary reasons for the indication of the allowability of the claim is the inclusions therein, in combination as currently claimed, of the limitation that wherein, at the controller via, the second metal layer comprises a separation barrier located adjacent the first metal layer and between the at least one resistor of the plural resistors and the controller bus is neither disclosed nor taught by the cited prior art of record, alone or in combination.

Referring to claims 17, 27: The primary reasons for the indication of the allowability of the claim is the inclusions therein, in combination as currently claimed, of the limitation that wherein the separation barrier comprises separation barrier portions within the power via and separation barrier portions within the controller via is neither disclosed nor taught by the cited prior art of record, alone or in combination.

Referring to claim 40: The primary reasons for the indication of the allowability of the claim is the inclusions therein, in combination as currently claimed, of the limitation that wherein the corrosion-resistive layer portion comprises a first separation barrier, between the control portion of the second conductive metal layer and the first portion of the first conductive metal layer at the control via is neither disclosed nor taught by the cited prior art of record, alone or in combination.

Claims 8 and 18-20 are allowed because they depend directly/indirectly on claim 2 or 17.

4. Claim 36 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The primary reasons for the indication of the allowability of the claim is the inclusions therein, in combination as currently claimed, of the limitation that the first metal layer

comprising a power bus and a FET bus and wherein the first and second electrical connections are made through the corrosion-resistant layer portion is neither disclosed nor taught by the cited prior art of record, alone or in combination.

5. Claims 37-39 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim 36 and any intervening claims.

Response to Arguments

Applicant's arguments filed 10/21/2004 have been fully considered but they are not persuasive.

Regarding to the arguments referring to claims 1, 10, 31, 33: The applicants argued that Kasamoto does not disclose "...the second metal layer comprises a separation barrier located adjacent the first metal layer and between the at least one resistor of the plural resistors and the power bus". As discussed above, Kasamoto's separation/corrosion barrier is the portion of layer 1103 (in the area 1105) sandwiched between layer *1110c* and layer *1110d* and located adjacent the first metal layer (*FIG. 1c, element 1110c*) and between the at least one resistor (*FIG. 1c, element 1102*) of the plural resistors and the power bus. In addition, the power is supplied to the thin film resistor 1102 through the separation barrier 1105. Therefore, Kasomoto discloses the above limitation.

Regarding to the arguments referring to claims 21, 31, 33: The applicants argued that Kasamoto does not disclose "...wherein the first metal layer is electrically connected to the electrical connection portion of the bottom layer portion at the via". Again, as shown in FIG. 1c, Kasamoto's first metal layer 1110c is electrically connected to the bottom layer 1103 at the via

1105. Therefore, Kasomoto discloses the above limitation.

In addition, the applicants argued that in Kasamoto, the "common lead electrode layer structure including an upper electrode layer 1110c and a lower electrode layer 1110b" is not disclosed as being a power bus and is not "a portion for providing power to a resistor". The examiner does not agree and the reason is that a common lead electrode, generally, is a part of a power-providing unit in an electrical/electronic device, because without connecting the common lead electrode to a load, power cannot be provided to the load. In other words, Kasamoto's common lead electrode is "a portion for providing power to a resistor" because without connecting the resistor to the common lead electrode, power cannot be provided to the resistor. Moreover, Kasamoto suggests that the common lead electrode layer is formed as individually separated conductive layers (patterned as a power bus) for each resistor 1102 (*column 7, lines 26-34*).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM S NGUYEN whose telephone number is (571)272-2151. The examiner can normally be reached on 7:00AM - 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, STEPHEN D MEIER can be reached on (571)272-2149. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
December 12, 2004

Hai Pham

HAI PHAM
PRIMARY EXAMINER